Intel® Pentium® II Xeon™ Processor Bus Terminator Design Guidelines

Release Date: July 1998

Order Number: 243774-001

CONTENTS

.

1. Overview

The Intel® Pentium® II Xeon™ processor includes termination circuitry for the microprocessor's Assisted Gunning Transceiver Logic (AGTL+) bus. In a multiple-processor system each processor location (Slot 2 connector) must be properly terminated, whether or not all locations have processors installed. This document describes design considerations for a termination card to occupy unused connector locations and terminate the bus.

These design guidelines include layout rules and hints based on system design experience. They do not define a specific card design nor constitute a specification. Card designers will still need an understanding of the system the card will be used in, as well as the customary simulation and system testing.

In the following four-way symmetric multi-processing (SMP) design example, all processor system bus AGTL+ signals are tied to +1.5V through a 150 W resistor, so that the bus maintains a 25 W impedance no matter what configuration is used in the five available slots. For a two-way SMP design (i.e. dual processor), the cluster controller connector is not needed. A two-way SMP design would simply have two processor locations and the 440GX AGPset or 450NX PCIset.

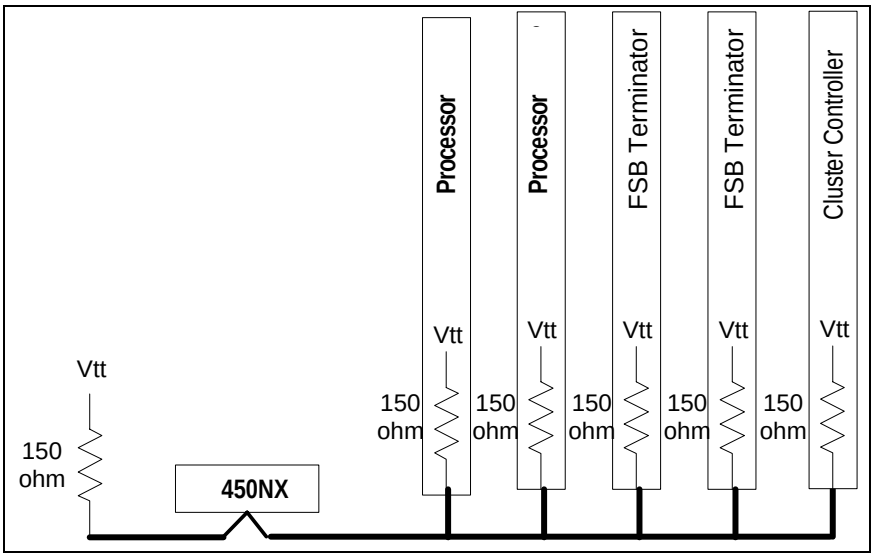

Figure 1. Processor System Bus Termination Example

2. Mechanical Specifications

2.1 Connector Interface

The Terminator Card uses a 330-pin gold finger connection to the processor baseboard Slot 2 connector. Below is the mechanical specification for the gold finger layout.

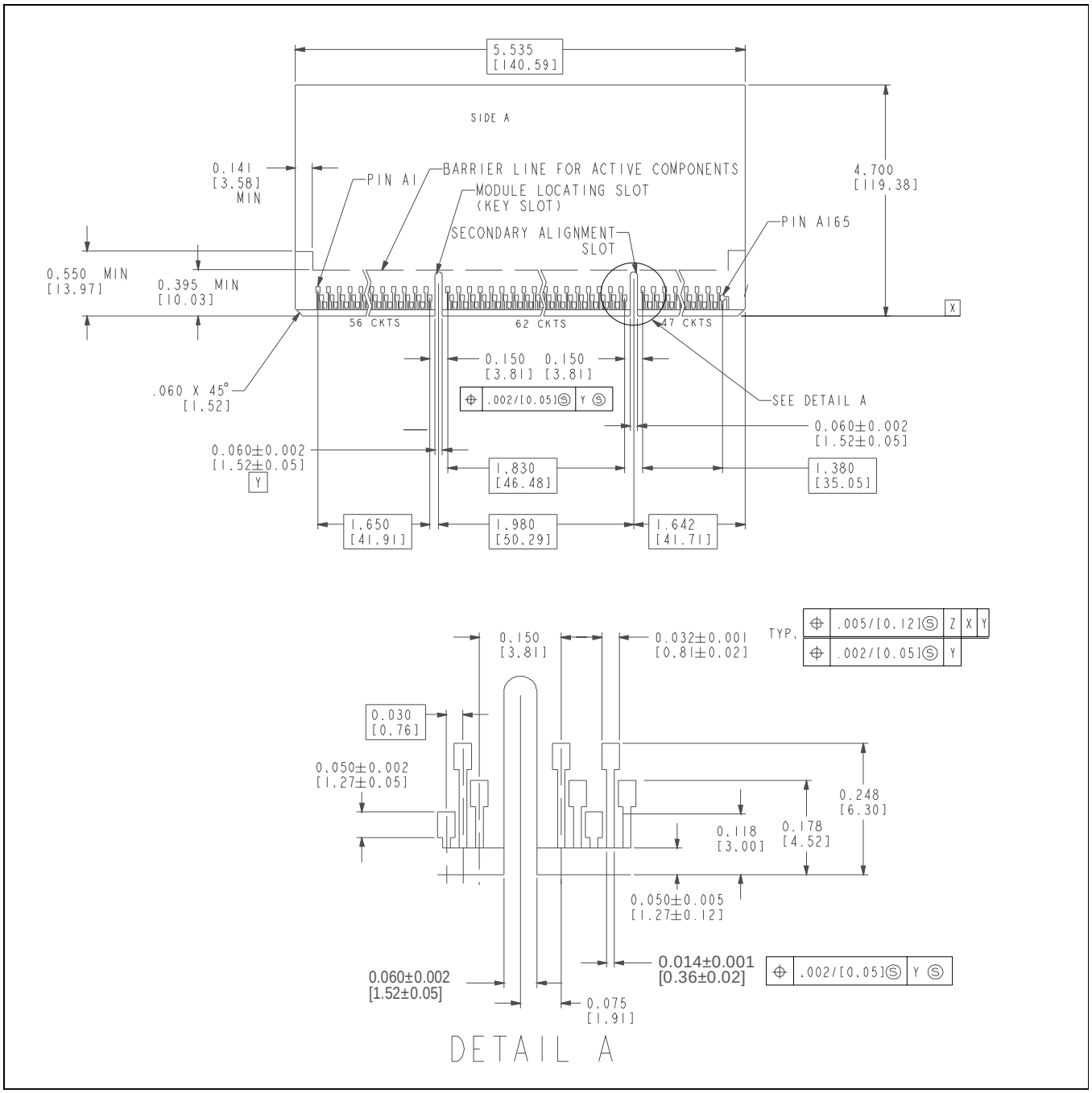

Figure 2. Interface Connector Pin Diagram, Primary Side

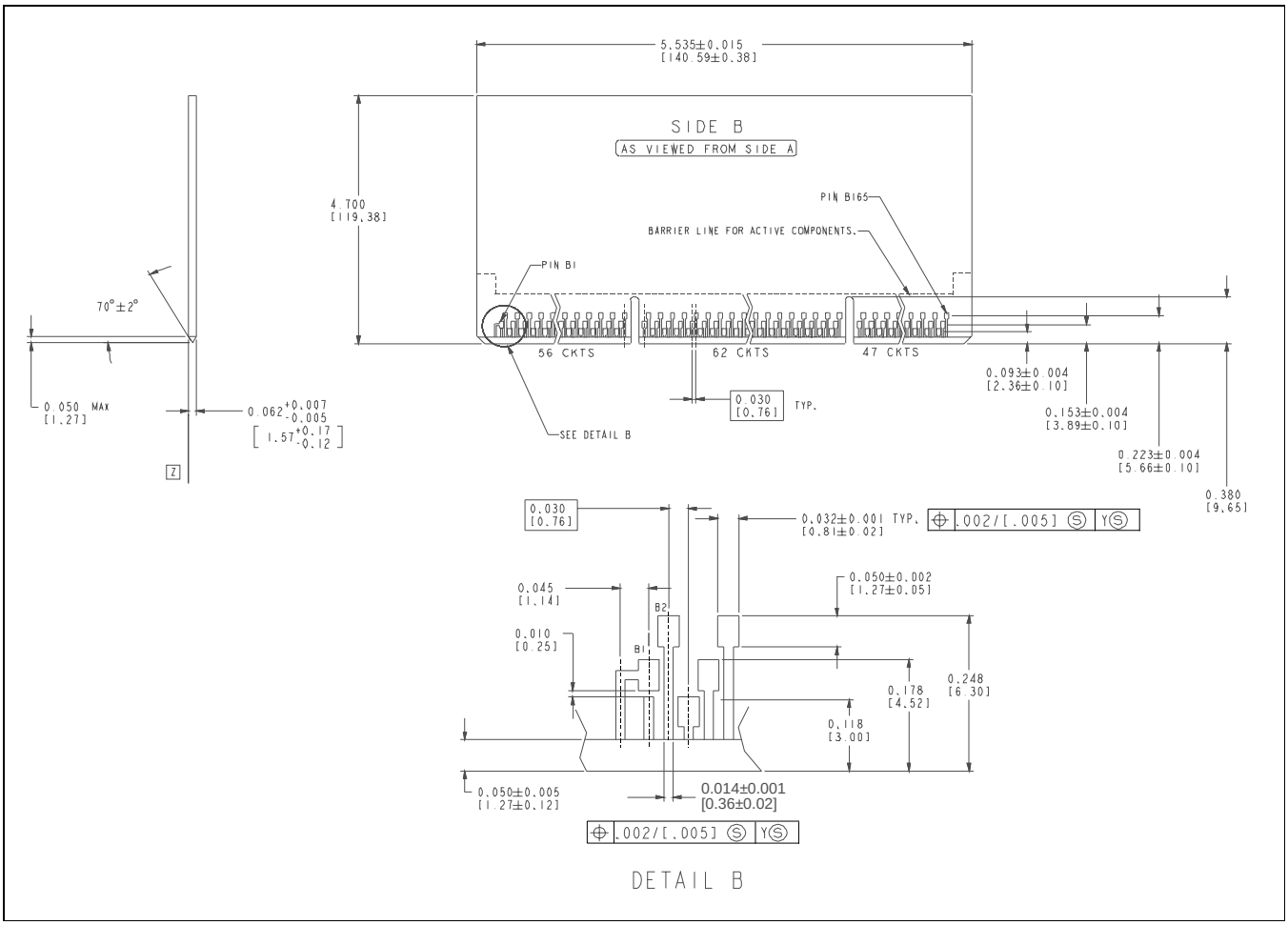

Figure 3. Interface Connector Pin Diagram, Secondary Side

2.1.1 Interface Pin Locations

Pin locations on the primary side, viewed from the primary side:

Upper row of gold fingers:		|	A1 A4 A7…
Middle row of gold fingers:	Board Edge →	|	A2 A5 A8…
Lower row of gold fingers:		|	A3 A6 A9…

Pin Locations on the secondary side, viewed from the secondary side:

Upper row of gold fingers:	…B8 B5 B2	|	
Middle Row of gold fingers:	…B7 B4 B1	|	← Board Edge
Lower row of gold fingers:	…B6 B3	|	

2.2 Mechanical Considerations

The bus terminator must mechanically fit into the Slot 2 connector, and also be retained during system shock and vibration. Normally the terminator PCB should mate with a housing or frame which emulates the top of the Pentium® II Xeon™ processor cartridge. The package emulation should allow the bus terminator to utilize any retention mechanism designed for the Pentium II Xeon processor.

3. Electrical Specifications

3.1 Power Requirements

The system baseboard must supply V_{tt} voltage to the pull-up resistors on the Terminator Card:

Table 1. DC Voltage

Voltage	1.5V ± 9 %	• Measured at substrate edge fingers • 1.5V ± 3% when bus is idle
Current	1.2 A	Maximum

3.2 Card Layout Guidelines

The design should follow AGTL+ layout guidelines:

- Use a trace routing length of 3.400 ± 0.032 inches to emulate the processor substrate's termination traces. Reducing this length may be beneficial for some topologies. Analog simulation should be performed to ensure the bus termination card does not cause any violation of signal integrity specifications (i.e. overshoot and undershoot).
- Distribute V_{tt} with a wide trace or plane. A four-layer board, with V_{tt} and ground planes as the internal layers, is preferred.
- If there are V_{tt} partial planes on either the top or the bottom layer, the widths of the planes should be ³ 200 mils. The partial planes should be stitched densely to the V_{tt} power plane.
- The V_{tt} end of terminating resistors should be connected to the V_{tt} plane with closely placed vias. Traces connecting the common pins of the V_{tt} end of the R-pack should be ³ 30 mils wide.
- Four sets of two edge finger pins connect to the V_{tt} plane on the top left, top right, bottom left, and bottom right. Each of the traces connecting the edge fingers to the V_{tt} plane should be ³ 12 mils wide and £ 200 mils long.
- Closely control the characteristic line impedance, Z_0, at 65 Ω ± 10%. A ground plane will be needed to maintain the proper characteristic line impedance.
- Use a PCB signal velocity of 2.05 to 2.15 ns/ft (stripline).
- Ensure that V_{tt} is decoupled correctly.
  - ◊ Traces connecting a capacitor pad to a via or component should be ³ 20 mils wide and £ 15 mils long.
  - ◊ There need to be at least two 47 mF capacitors on the card. One should be placed to the left and one to the right (top or bottom), adjacent to the V_{tt}-pin traces.
  - ◊ Connect one 1 uF capacitor directly to the V_{tt} end of each R-pack (or equivalent group of discrete resistors). Also for every two R-packs, place one 0.1 uF capacitor next to the R-packs.
- Take steps to minimize crosstalk:
  - ◊ Maximize the line-to-line spacing (minimum three width spacing to one width trace). Leave at least 15 mils between traces.
  - ◊ Keep the dielectric constant of the termination card between 4.2 and 4.8.
  - ◊ Minimize the cross-sectional area of the traces (5 mil lines with 1 ounce/ft ^{2} copper – but beware of higher-resistivity traces).
  - ◊ Eliminate parallel traces between layers if not separated by a power or ground plane.

- ◊ Isolate AGTL+ signals in groups. That is, route the data signals in one group, the control signals in one group, and the address signals in another group. If the groups are routed together on a plane, provide at least 25 mils separation between the groups.

- Conventional "pull-up" resistor networks may not be suitable for termination. These networks have a common power or ground pin at the extreme end of the package, shared by 13 to 19 resistors (for 14- and 20-pin components). These packages generally have too much inductance to maintain the voltage and current needed at each resistive load. For better results, use discrete resistors, resistor packages with two separate pins for each resistor, or other resistor networks with acceptable characteristics.

The design should follow these guidelines in addition to the AGTL+ layout rules:

- The PWR_EN trace must be ³ 15 mils wide.

- BCLK termination may be necessary in some systems, using a 2-inch trace to a pad to allow addition of a capacitor (probably about 10 pF) if system testing shows it is necessary.

3.3 Interface Pinout

The tables on the following pages list the connections on the Terminator Card for each pin. Each line on the table lists:

- Pin number
- Signal name, if used by the Terminator Card
- Connection on the card

Pins designated "N/C" should be open — not connected to any trace or plane on the terminator card.

Table 2. Interface Connector Pinout

Pin	Signal	Connects to:	Pin	Signal	Connects to:	Pin	Signal	Connects to:
A1	N/C		A56	N/C		A111	GROUND	
A2	N/C		A57	GROUND		A112	A#(19)	150 Ω to V_{tt}
A3	N/C		A58	D#(42)	150 Ω to V_{tt}	A113	A#(18)	150 Ω to V_{tt}
A4	GROUND		A59	D#(45)	150 Ω to V_{tt}	A114	GROUND	
A5	+1.5V		A60	GROUND		A115	A#(16)	150 Ω to V_{tt}
A6	+1.5V		A61	D#(39)	150 Ω to V_{tt}	A116	A#(13)	150 Ω to V_{tt}
A7	GROUND		A62	N/C		A117	GROUND	
A8	N/C		A63	GROUND		A118	A#(14)	150 Ω to V_{tt}
A9	N/C		A64	D#(43)	150 Ω to V_{tt}	A119	GROUND	
A10	GROUND		A65	D#(37)	150 Ω to V_{tt}	A120	A#(10)	150 Ω to V_{tt}
A11	N/C		A66	GROUND		A121	A#(5)	150 Ω to V_{tt}
A12	N/C		A67	D#(33)	150 Ω to V_{tt}	A122	GROUND	
A13	GROUND		A68	D#(35)	150 Ω to V_{tt}	A123	A#(9)	150 Ω to V_{tt}
A14	N/C		A69	GROUND		A124	A#(4)	150 Ω to V_{tt}
A15	N/C		A70	D#(31)	150 Ω to V_{tt}	A125	GROUND	
A16	GROUND		A71	D#(30)	150 Ω to V_{tt}	A126	N/C	
A17	N/C		A72	GROUND		A127	BNR#	150 Ω to V_{tt}
A18	TEST	A20	A73	D#(27)	150 Ω to V_{tt}	A128	GROUND	
A19	GROUND		A74	D#(24)	150 Ω to V_{tt}	A129	BPRI#	150 Ω to V_{tt}
A20	TEST	A18	A75	GROUND		A130	TRDY#	150 Ω to V_{tt}
A21	N/C		A76	D#(23)	150 Ω to V_{tt}	A131	GROUND	
A22	GROUND		A77	D#(21)	150 Ω to V_{tt}	A132	DEFER#	150 Ω to V_{tt}
A23	N/C		A78	GROUND		A133	REQ#(2)	150 Ω to V_{tt}
A24	N/C		A79	D#(16)	150 Ω to V_{tt}	A134	GROUND	
A25	GROUND		A80	D#(13)	150 Ω to V_{tt}	A135	REQ#(3)	150 Ω to V_{tt}
A26	N/C		A81	GROUND		A136	HITM#	150 Ω to V_{tt}
A27	N/C		A82	TESTHI	150 Ω to V_{tt}	A137	GROUND	
A28	GROUND		A83	N/C		A138	DBSY#	150 Ω to V_{tt}
A29	N/C		A84	GROUND		A139	RS#(1)	150 Ω to V_{tt}

'Pin	Signal	Connects to:	Pin	Signal	Connects to:	Pin	Signal	Connects to:
A30	N/C		A85	D#(11)	150 Ω to V_{tt}	A140	GROUND	
A31	GROUND		A86	D#(10)	150 Ω to V_{tt}	A141	BREQ#(2)	150 Ω to V_{tt}
A32	N/C		A87	GROUND		A142	BREQ#(0)	150 Ω to V_{tt}
A33	N/C		A88	D#(14)	150 Ω to V_{tt}	A143	GROUND	
A34	GROUND		A89	D#(9)	150 Ω to V_{tt}	A144	ADS#	150 Ω to V_{tt}
A35	BINIT#	150 Ω to V_{tt}	A90	GROUND		A145	AP#(0)	150 Ω to V_{tt}
A36	DEP#(0)	150 Ω to V_{tt}	A91	D#(8)	150 Ω to V_{tt}	A146	GROUND	
A37	GROUND		A92	D#(5)	150 Ω to V_{tt}	A147	N/C	
A38	(DEP#(1)	150 Ω to V_{tt}	A93	GROUND		A148	N/C	
A39	(DEP#(3)	150 Ω to V_{tt}	A94	D#(3)	150 Ω to V_{tt}	A149	GROUND	
A40	GROUND		A95	D#(1)	150 Ω to V_{tt}	A150	N/C	
A41	DEP#(5)	150 Ω to V_{tt}	A96	GROUND		A151	N/C	
A42	DEP#(6)	150 Ω to V_{tt}	A97	BCLK	2” trace to pad	A152	GROUND	
A43	GROUND		A98	N/C		A153	L2_VID(2)	(OPEN)
A44	D#(61)	150 Ω to V_{tt}	A99	GROUND		A154	L2_VID(1)	(OPEN)
A45	D#(55)	150 Ω to V_{tt}	A100	BERR#	150 Ω to V_{tt}	A155	GROUND	
A46	GROUND		A101	A#(33)	150 Ω to V_{tt}	A156	+1.5V	
A47	D#(60)	150 Ω to V_{tt}	A102	GROUND		A157	+1.5V	
A48	D#(53)	150 Ω to V_{tt}	A103	A#(34)	150 Ω to V_{tt}	A158	GROUND	
A49	GROUND		A104	A#(30)	150 Ω to V_{tt}	A159	N/C	
A50	D#(57)	150 Ω to V_{tt}	A105	GROUND		A160	N/C	
A51	D#(46)	150 Ω to V_{tt}	A106	A#(31)	150 Ω to V_{tt}	A161	GROUND	
A52	GROUND		A107	A#(27)	150 Ω to V_{tt}	A162	N/C	
A53	D#(49)	150 Ω to V_{tt}	A108	GROUND		A163	N/C	
A54	D#(51)	150 Ω to V_{tt}	A109	A#(22)	150 Ω to V_{tt}	A164	GROUND	
A55	GROUND		A110	A#(23)	150 Ω to V_{tt}	A165	PWR_EN(0)	Pin B1

Pin	Signal	Connects to:	Pin	Signal	Connects to:	Pin	Signal	Connects to:
B1	PWR_EN(1)	Pin A165	B56	N/C		B111	A#(21)	150 Ω to V_{tt}
B2	N/C		B57	N/C		B112	N/C	
B3	N/C		B58	N/C		B113	A#(25)	150 Ω to V_{tt}
B4	N/C		B59	D#(41)	150 Ω to V_{tt}	B114	A#(15)	150 Ω to V_{tt}
B5	N/C		B60	D#(47)	150 Ω to V_{tt}	B115	N/C	
B6	+1.5V		B61	N/C		B116	A#(17)	150 Ω to V_{tt}
B7	+1.5V		B62	D#(44)	150 Ω to V_{tt}	B117	A#(11)	150 Ω to V_{tt}
B8	N/C		B63	D#(36)	150 Ω to V_{tt}	B118	N/C	
B9	N/C		B64	N/C		B119	A#(12)	150 Ω to V_{tt}
B10	N/C		B65	D#(40)	150 Ω to V_{tt}	B120	N/C	
B11	N/C		B66	D#(34)	150 Ω to V_{tt}	B121	A#(8)	150 Ω to V_{tt}
B12	N/C		B67	N/C		B122	A#(7)	150 Ω to V_{tt}
B13	N/C		B68	D#(38)	150 Ω to V_{tt}	B123	N/C	
B14	N/C		B69	D#(32)	150 Ω to V_{tt}	B124	A#(3)	150 Ω to V_{tt}
B15	N/C		B70	N/C		B125	A#(6)	150 Ω to V_{tt}
B16	N/C		B71	D#(28)	150 Ω to V_{tt}	B126	N/C	
B17	N/C		B72	D#(29)	150 Ω to V_{tt}	B127	AERR#	150 Ω to V_{tt}
B18	N/C		B73	N/C		B128	REQ#(0)	150 Ω to V_{tt}
B19	N/C		B74	D#(26)	150 Ω to V_{tt}	B129	N/C	
B20	N/C		B75	D#(25)	150 Ω to V_{tt}	B130	REQ#(1)	150 Ω to V_{tt}
B21	N/C		B76	N/C		B131	REQ#(4)	150 Ω to V_{tt}
B22	N/C		B77	D#(22)	150 Ω to V_{tt}	B132	N/C	
B23	N/C		B78	D#(19)	150 Ω to V_{tt}	B133	LOCK#	150 Ω to V_{tt}
B24	N/C		B79	N/C		B134	DRDY#	150 Ω to V_{tt}
B25	N/C		B80	D#(18)	150 Ω to V_{tt}	B135	N/C	
B26	N/C		B81	D#(20)	150 Ω to V_{tt}	B136	RS#(0)	150 Ω to V_{tt}
B27	N/C		B82	N/C		B137	HIT#	150 Ω to V_{tt}
B28	N/C		B83	N/C		B138	N/C	
B29	N/C		B84	N/C		B139	RS#(2)	150 Ω to V_{tt}
B30	N/C		B85	N/C		B140	RP#	150 Ω to V_{tt}
B31	N/C		B86	D#(17)	150 Ω to V_{tt}	B141	N/C	
B32	N/C		B87	D#(15)	150 Ω to V_{tt}	B142	BREQ#(3)	150 Ω to V_{tt}
B33	N/C		B88	N/C		B143	BREQ#(1)	150 Ω to V_{tt}
B34	N/C		B89	D#(12)	150 Ω to V_{tt}	B144	N/C	
B35	N/C		B90	D#(7)	150 Ω to V_{tt}	B145	RSP#	150 Ω to V_{tt}
B36	N/C		B91	N/C		B146	AP#(1)	150 Ω to V_{tt}
B37	N/C		B92	D#(6)	150 Ω to V_{tt}	B147	N/C	
B38	N/C		B93	D#(4)	150 Ω to V_{tt}	B148	N/C	
B39	(DEP#(2)	150 Ω to V_{tt}	B94	N/C		B149	N/C	
B40	(DEP#(4)	150 Ω to V_{tt}	B95	D#(2)	150 Ω to V_{tt}	B150	N/C	
B41	N/C		B96	D#(0)	150 Ω to V_{tt}	B151	N/C	
B42	(DEP#(7)	150 Ω to V_{tt}	B97	N/C		B152	L2_VID(0)	(OPEN)
B43	D#(62)	150 Ω to V_{tt}	B98	P6_RESET_L	150 Ω to V_{tt}	B153	N/C	
B44	N/C		B99	N/C		B154	L2_VID(4)	GROUND
B45	D#(58)	150 Ω to V_{tt}	B100	N/C		B155	L2_VID(3)	(OPEN)
B46	D#(63)	150 Ω to V_{tt}	B101	A#(35)	150 Ω to V_{tt}	B156	N/C	
B47	N/C		B102	A#(32)	150 Ω to V_{tt}	B157	+1.5V	
B48	D#(56)	150 Ω to V_{tt}	B103	N/C		B158	+1.5V	
B49	D#(50)	150 Ω to V_{tt}	B104	A#(29)	150 Ω to V_{tt}	B159	N/C	
B50	N/C		B105	A#(26)	150 Ω to V_{tt}	B160	N/C	
B51	D#(54)	150 Ω to V_{tt}	B106	N/C		B161	N/C	
B52	D#(59)	150 Ω to V_{tt}	B107	A#(24)	150 Ω to V_{tt}	B162	N/C	
B53	N/C		B108	A#(28)	150 Ω to V_{tt}	B163	N/C	
B54	D#(48)	150 Ω to V_{tt}	B109	N/C		B164	N/C	
B55	D#(52)	150 Ω to V_{tt}	B110	A#(20)	150 Ω to V_{tt}	B165	N/C	

Appendix: Indicating Presence of Processor or Terminator Card in Connector

1. Power Enable Link

   The processor indicates its presence by connecting the two PWR_EN signals on pins B1 and A165. The Terminator Card should connect these two pins to allow the system to check continuity and verify that either a processor or Terminator Card is properly inserted in the socket.

2. VRM Voltage Identification Bits

   To allow the system to correctly detect that a Terminator Card (instead of the Pentium® II Xeon™ processor) is installed in a particular processor slot, some systems look for the Voltage Identification (VID) bit pattern. The example below uses the L2 cache VID bits. Refer to the Intel Pentium II Xeon processor data sheet for the rest of the possible VID combinations.

Table A. L2 Cache VRM Voltage Identification (VID_{L2}) Bits

Processor L2 Cache Pins 0 = Connected to Vss 1= Open or pull-up to Vin					
VID4	**VID3**	**VID2**	**VID1**	**VID0**	
0	1	1	1	1	**Terminator present**

UNITED STATES, Intel Corporation
2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA 95052-8119
Tel: +1 408 765-8080

JAPAN, Intel Japan K.K.
5-6 Tokodai, Tsukuba-shi, Ibaraki-ken 300-26
Tel: + 81-29847-8522

FRANCE, Intel Corporation S.A.R.L.
1, Quai de Grenelle, 75015 Paris
Tel: +33 1-45717171

UNITED KINGDOM, Intel Corporation (U.K.) Ltd.
Pipers Way, Swindon, Wiltshire, England SN3 1RJ
Tel: +44 1-793-641440

GERMANY, Intel GmbH
Dornacher Strasse 1
85622 Feldkirchen/ Muenchen
Tel: +49 89/99143-0

HONG KONG, Intel Semiconductor Ltd.
32/F Two Pacific Place, 88 Queensway, Central
Tel: +852 2844-4555

CANADA, Intel Semiconductor of Canada, Ltd.
190 Attwell Drive, Suite 500
Rexdale, Ontario M9W 6H8
Tel: +416 675-2438